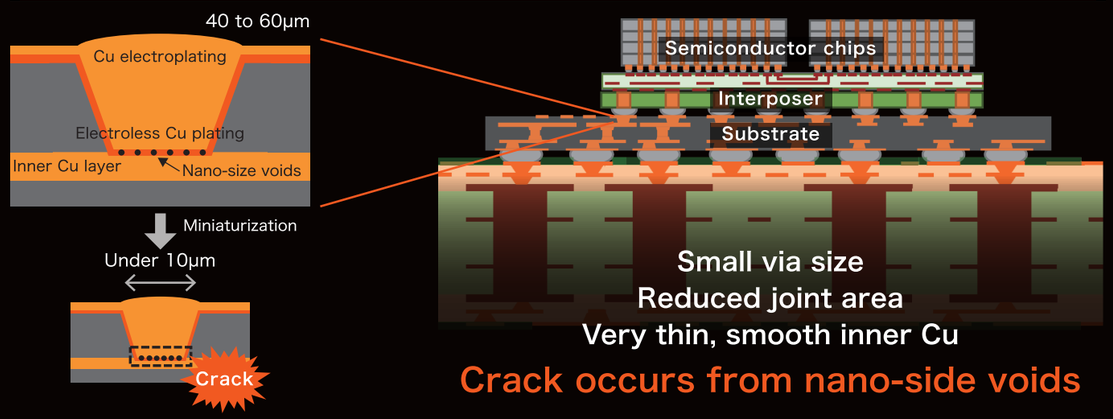
OPC FLET PROCESS

SAP

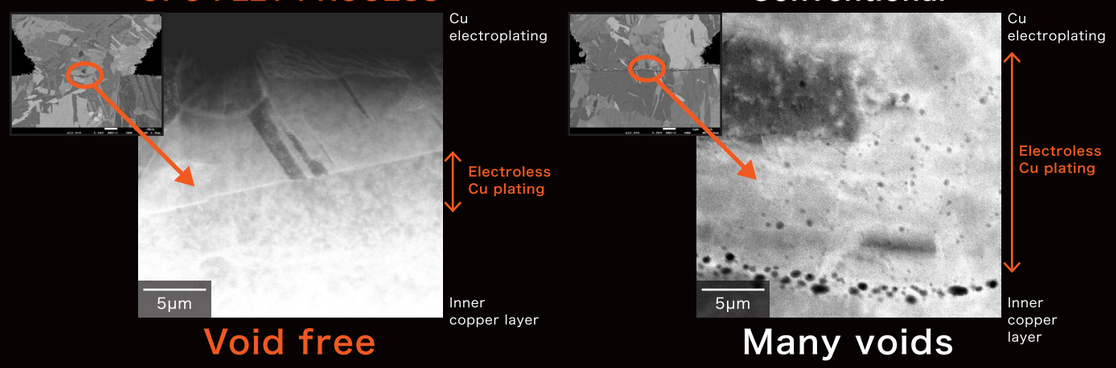
Electroless copper plating process to solve Weak-Micro Via For high connection reliability

- Realize crystal continuity, prevent nano voids
- High connection reliability at via bottom
- High throwing power by small thickness
- High peel strength even on low profile substrates
- Uniform and thin seed layers, excellent in pattern formation

For high density patterning in substrates

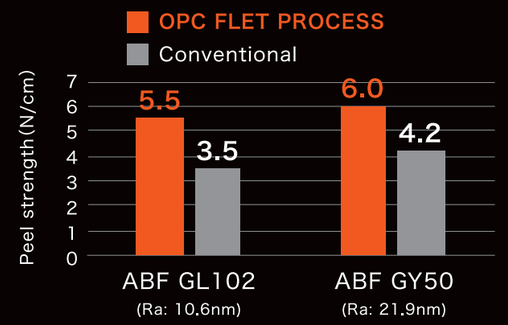


High purity, small thickness for via-bottom void free

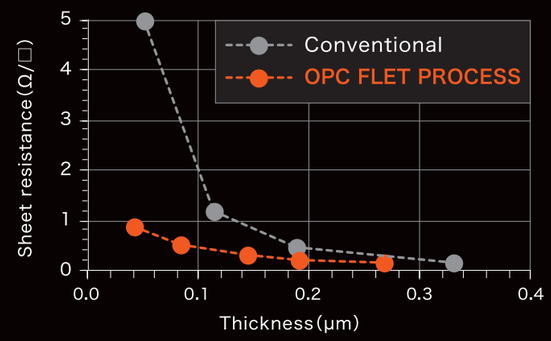


Presented by SANKEN, Osaka University Flexible 3D JISSO Collaborative Research Institute

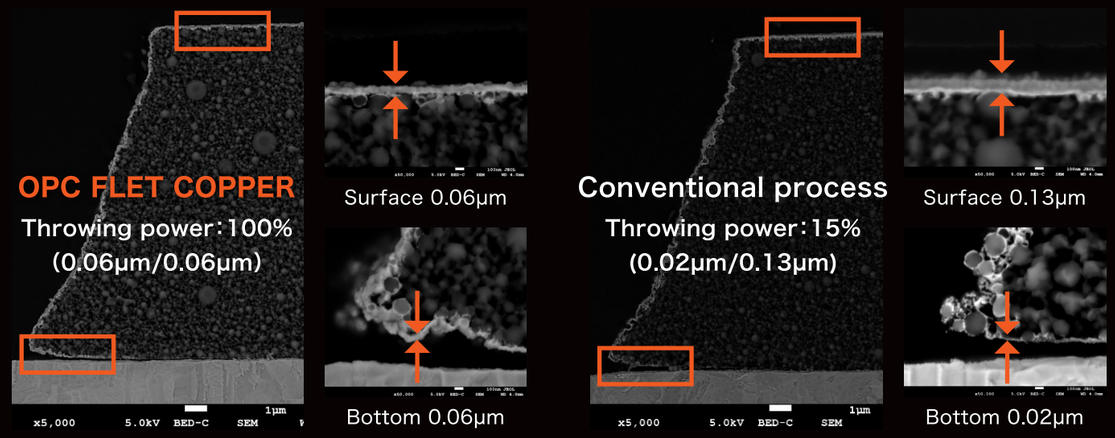
High peel strength on low profile substrates



Low resistance value by small thickness

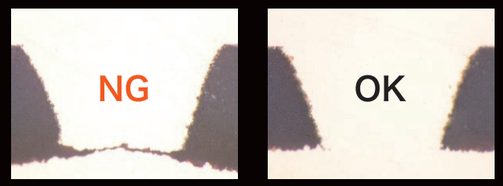


High via coverage with small thickness



High connection reliability at via bottom

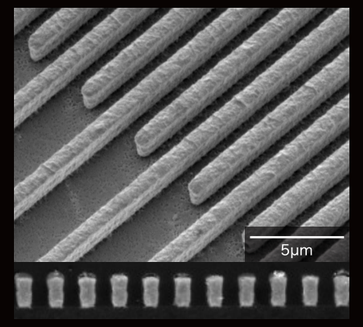
- Solder heat resistance test : 293℃, dipping for 10 s, 10 cycles
- Solder : Sn-Cu solder
- ABF GL102, via diameter 80μm



NG mode／Number of observed vias	Soft-etching amount in electroless Cu plating step (μm)		
	0	0.05	1.0
Conventional	16/100	10/100	0/100
OPC FLET PROCESS	0/100	0/100	0/100

Ultra-fine patterning

Achieve L/S=1/1μm



After seed layer etching

Reduce seed layer thickness
Improve fine pattern performance

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