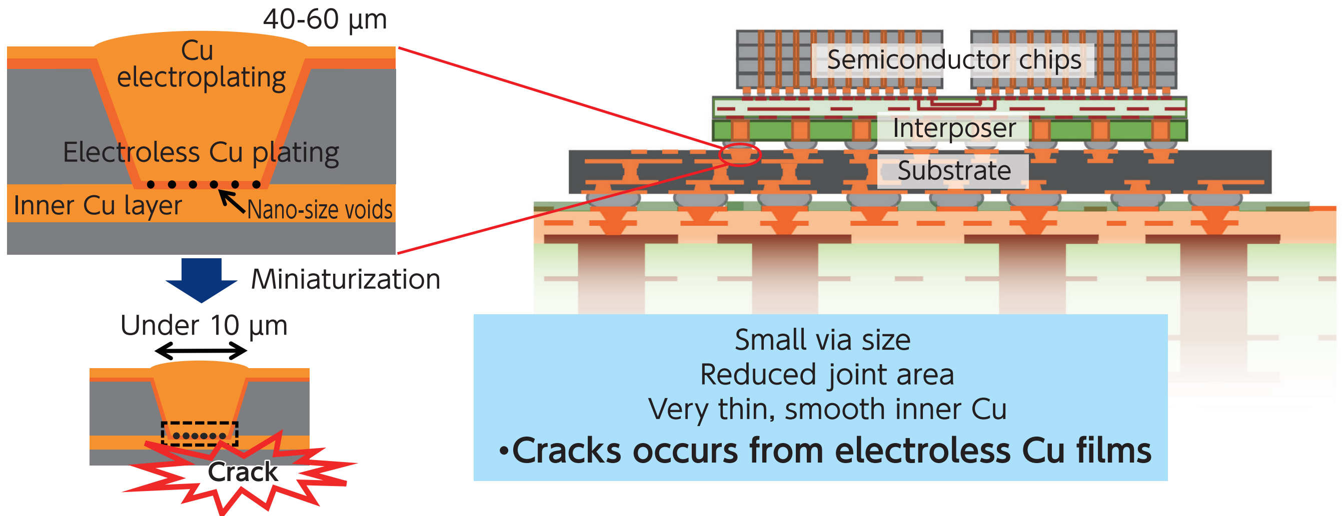
Electroless copper plating process to solve Weak-Micro Via

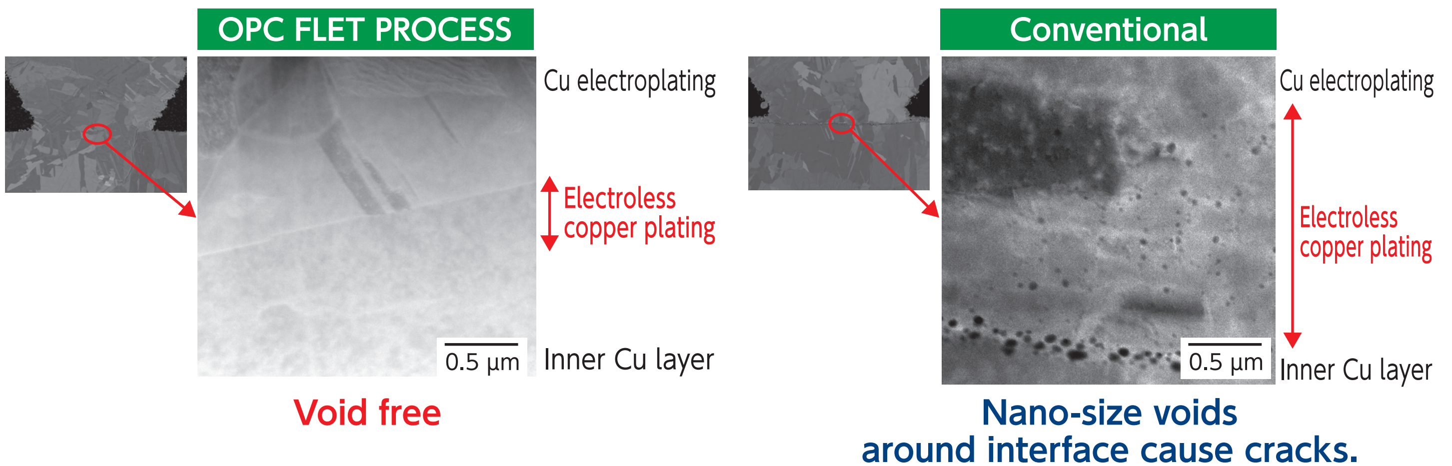
OPC FLET PROCESS

SAP

Current problem of IC substrate



High Cu purity, small thickness for via-bottom void free

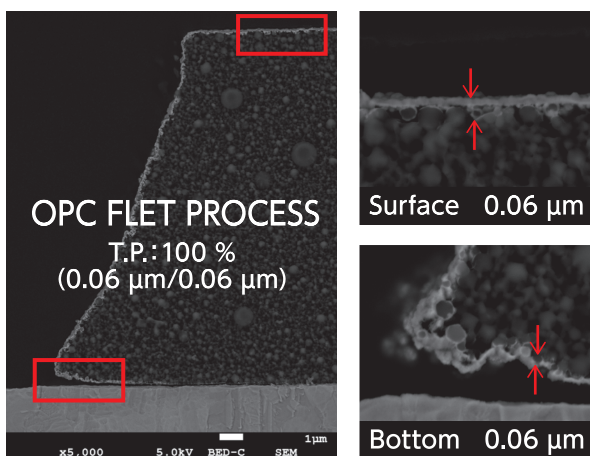


Void free

Nano-size voids around interface cause cracks.

Presented by SANKEN, Osaka University Flexible 3D JISSO Collaborative Research Institute

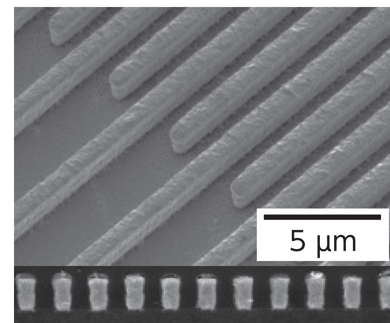
High covering power by small thickness



Reduced thickness of seed layer

Ultra-fine pattern formation

Achieve L/S=1/1 μm



After seed etching

Fine pattern formation by thickness reduction