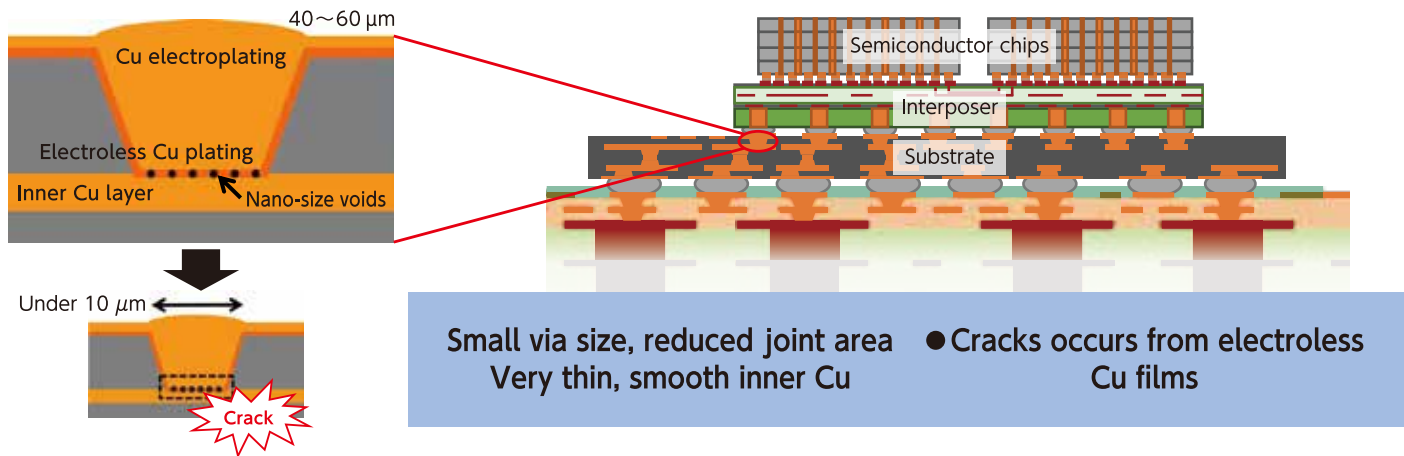


Electroless copper plating process to solve Weak-Micro Via

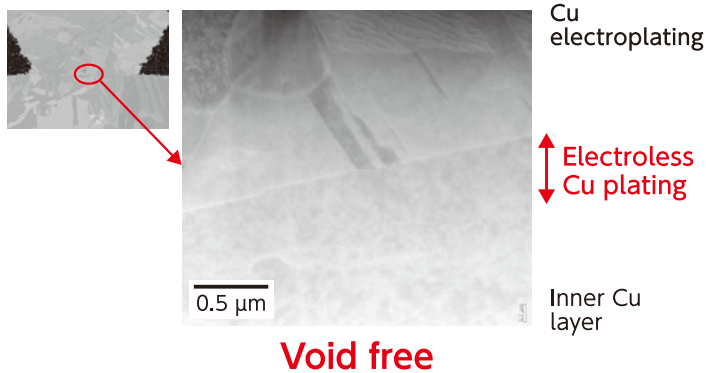
OPC FLET PROCESS

Current problem of IC substrate

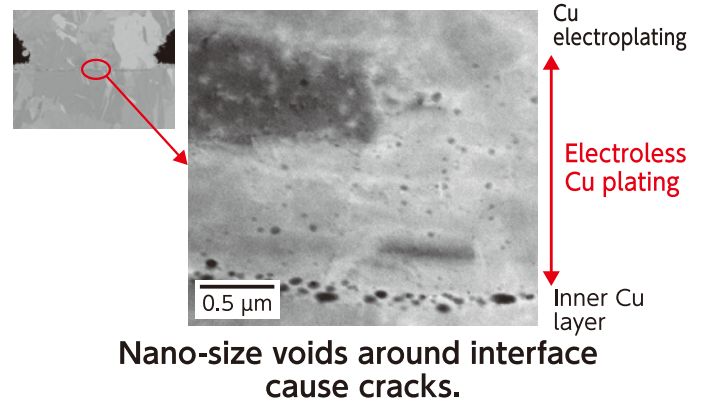


High Cu purity, small thickness for via-bottom void free

OPC FLET PROCESS

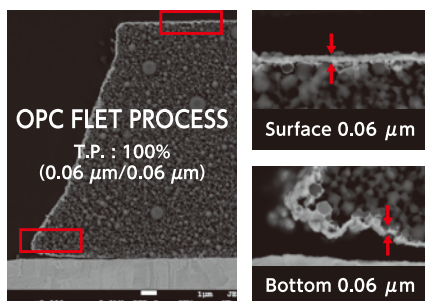


Conventional



Presented by SANKEN, Osaka University Flexible 3D JISSO Collaborative Research Institute

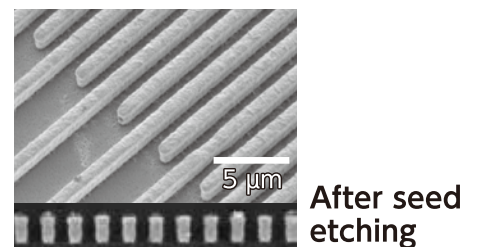
High covering power by small thickness



Reduced thickness of seed layer

Ultra-fine pattern formation

Achieve L/S=1/1 μm



Fine pattern formation by thickness reduction

